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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/904,663	07/16/2001	Mikio Ohtaki	KAN 120D1	7934

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EXAMINER	
HOLLINGTON, JERMELE M	
ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 12/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/904,663	OHTAKI, MIKIO	
	Examin r	Art Unit	
	Jermele M. Hollington	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 September 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-27 and 42-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-27 and 42-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/434,490.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *08/03* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 21-27 and 42-52 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Regarding claims 21, 42-44 and 51-52, the claim recites: "...the back or second surface of the wafer exposed to convective air in the burn-in apparatus..." The specification does not in a clear, concise and full description describe the above claim limitation. On page 23, lines 25-30, it describes a ventilating through holes in the hold pate to help circulate air to the expose wafer. However, it does not describe that the air is being exposed to the back surface of the wafer as claimed.

For examination purposes, the examiner is not giving patentable weight to the limitation "the back surface of the wafer exposed to convective air" until further explanation is given of this limitation in the claim. Since claims 22-27 depend off of claim 21 and claims 45-52 depend off of claim 44, they are also rejected.

Regarding claims 24, 26, 47 and 49, the claim recites: "...disposing over the back or second surface of the wafer a holding plate having a through hole..." The specification does not

in a clear, concise and full description describe the above claim limitation. On page 23, lines 25-30, it describes a ventilating through holes in the hold pate to help circulate air to the expose wafer. However, it does not describe that the holding plate is being dispose over the back surface of the wafer as claimed.

For examination purposes, the examiner is not giving patentable weight to the limitation "the back surface of the wafer" until further explanation is given of this limitation in the claim. Since claim 42 depends off of claim 24, claim 43 depends off of claim 26, claim 51 depends off of claim 47 and claim 52 depends off of claim 49, they are also rejected.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 21-27 are 42-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakata et al (6297658) in view of Budnaitis et al (5896038).

Regarding claim 21, Nakata et al discloses [see fig. 1] a method of manufacturing probe card of a wafer burn-in cassette comprising providing a semiconductor wafer (10) with a front surface (top surface of the wafer) having a plurality of circuit elements (semiconductor chips) [see col. 6, lines 25-26] formed thereon [see column 3 lines 27-30 and column 6 lines 25-26], where the semiconductor wafer (10) has a back surface (bottom of wafer) opposite to the front surface (top surface), forming on the front surface (top surface) a plurality of electrodes (16) connected with the circuit elements (semiconductor chips) [see column 6 lines 30-31], coating

the wafer surface with a resin film (represented as probe card 12) [see column 6 lines 27-28], the plurality of electrodes (16)being exposed through the resin film (12) [see fig. 1], inserting the wafer (10) into a burn-in apparatus (represented as burn-in cassette), testing the plurality of circuit elements [not shown] for electrical functions in the burn-in apparatus (burn-in cassette) through the plurality of electrodes (16) and dividing the wafer (10) [see fig. 3 with scribe lines dividing each semiconductor device] into the plurality of semiconductor device [not number but shown in fig. 3]. However, he does not disclose the wafer expose to air as claimed. Budnaitis et al disclose [see Figs. 2-3] providing a semiconductor wafer (1) with a wafer surface having a plurality of circuit elements (chips 2) formed thereon, inserting the wafer (1) into a burn-in apparatus (6) wherein the wafer (1) is exposed to convective air in the burn-in apparatus (6) [see column 8 lines 41-54]. Further, Budnaitis et al teach that the addition of the wafer exposed to air is advantageous because it provides temperature control of the wafer during testing in the burn-in apparatus. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Nakata et al by adding means to blow air on the wafer as taught by Budnaitis in order to control the temperature of the wafer during testing in the burn-in apparatus.

Regarding claims 22, Nakata inherently discloses dividing the wafer after testing [see fig. 3].

Regarding claims 23 and 25, Nakata discloses mounting the wafer (10) on a circuit board (represented as wiring board 13) with an elastic sheet or film (represented as conductive rubber 21) interposed there between including electrically connecting wiring circuit [nit number but

shown in fig. 1] on the circuit board (13) to the electrodes (16) on the wafer (10) through bump electrode (17) in the film (21).

Regarding claims 24 and 26, Nakata discloses disposing over the wafer (10) a holding plate (represented as first sealed member 15 and second sealed member 25) having a through hole (26) and pressing the wafer (10) on the circuit board (13) with the holding plate (15 and 25) [see column 6 line 56- column 7 line 54].

Regarding claim 27, Nakata discloses forming a plurality of solder balls as the electrodes (17) [see fig. 1].

Regarding claims 42-43, Budnaitis et al disclose [see Figs. 2-3] providing the convective air (hot or cold) over the wafer (1) through a through hole [see column 8 lines 41-52].

Regarding claim 44, Nakata et al discloses [see fig. 1] a method of manufacturing probe card of a wafer burn-in cassette comprising preparing a semiconductor wafer (10) with a first surface (top surface) and a second surface (bottom surface), the second surface being opposite to the first surface, wherein the first surface has a plurality of circuit elements (semiconductor chips) [not shown] formed thereon [see column 3 lines 27-30 and column 6 lines 25-26], forming a plurality of electrodes (16) on the first surface, the electrodes (16) being connected to the circuit elements [see column 6 lines 30-31], inserting the wafer (10) into a burn-in apparatus (represented as burn-in cassette), testing the plurality of circuit elements [not shown] for electrical functions in the burn-in apparatus (burn-in cassette) through the plurality of electrodes (16) and dividing the wafer (10) [see fig. 3 with scribe lines dividing each semiconductor device] into the plurality of semiconductor device [not number but shown in fig. 3]. However, he does not disclose the wafer expose to air as claimed. Budnaitis et al disclose [see Figs. 2-3] providing

a semiconductor wafer (1) with a wafer surface having a plurality of circuit elements (chips 2) formed thereon, inserting the wafer (1) into a burn-in apparatus (6) wherein the wafer (1) is exposed to convective air in the burn-in apparatus (6) [see column 8 lines 41-52]. Further, Budnaitis et al teach that the addition of the wafer exposed to air is advantageous because it provides temperature control of the wafer during testing in the burn-in apparatus. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Nakata et al by adding means to blow air on the wafer as taught by Budnaitis et al in order to control the temperature of the wafer during testing in the burn-in apparatus.

Regarding claims 45, Nakata inherently discloses dividing the wafer after testing [see fig. 3].

Regarding claims 46 and 48, Nakata discloses mounting the wafer (10) on a circuit board (represented as wiring board 13) with an elastic sheet or film (represented as conductive rubber 21) interposed there between including electrically connecting wiring circuit [nit number but shown in fig. 1] on the circuit board (13) to the electrodes (16) on the wafer (10) through bump electrode (17) in the film (21).

Regarding claims 47 and 49, Nakata discloses disposing over the wafer (10) a holding plate (represented as first sealed member 15 and second sealed member 25) having a through hole (26) and pressing the wafer (10) on the circuit board (13) with the holding plate (15 and 25) [see column 6 line 56- column 7 line 54].

Regarding claim 50, Nakata discloses forming a plurality of solder balls as the electrodes (17) [see fig. 1].

Regarding claims 51-52, Budnaitis et al disclose [see Figs. 2-3] providing the convective air over the wafer (1) through a through hole [see column 8, lines 41-52].

Conclusion

5. Applicant's arguments filed Sept. 4, 2003 have been fully considered but they are not persuasive.

Regarding claims 21 and 44, the applicant states: "...However, as the Examiner acknowledges in the Office Action, Nakata fails to disclose exposing the **rear surface** of the semiconductor wafer 10 to air circulation..."

The examiner agrees with the applicant except that the examiner only acknowledged that Nakata fails to disclose exposing the wafer to air circulation and not the rear surface of the wafer as indicated above.

Further, the applicant states: "...However, Budnaitis fails to disclose cooling by exposing the back surface of the wafer to convective air in the burn-in apparatus...The forced air circulation suggested in Budnaitis is significantly different from the convective cooling claimed in the present invention...neither of the references teaches or suggests exposing the back surface to convective air in the burn apparatus..."

In response to the above arguments, the examiner has not given patentable weight to the limitation "back surface" since there is no description given in the specification that the back of the wafer is being exposed to air as claimed. Furthermore, the applicant has not provided a description of convective to determine that the air circulation of the present invention is different from the air circulation of the prior art. Therefore, the arguments are not persuasive.

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (703) 305-1653. The examiner can normally be reached on M-F (9:00-4:30 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (703) 308-1233. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Jermele M. Hollington
Examiner
Art Unit 2829

JMH
November 20, 2003

David A. Zarneke
Primary Exmr
11/25/3